007
12-14-07

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L2	98	pipeline near2 accelerator	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L3	1038	pipeline with accelerat$3	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L4	261	pipeline near2 accelerat$3	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L5	47	pipeline near2 accelerat$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L6	2	accelerat$3 with load$3 with process$3 with external and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L7	71	accelerat$3 with load$3 with process$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L8	3	("5583964" "4956771" "5892962").pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L9	10	mccarthy-paul.in.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L10	1	"5619430".pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L11	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L12	8	"raw data" with (coprocessor co-processor) same (buffer queue FIFO)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L13	42	"raw data" with (coprocessor co-processor)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L14	208	"raw data" with (slave PE DSP)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L15	9	"raw data" with (slave PE DSP) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L16	19	"processed data" with (coprocessor co-processor) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L17	1	(US-6624819-$).did.	USPAT	OR	ON	2007/12/14 11:38
L18	1	L17 and "160" with ("204" "206")	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L19	193	output near2 queue with (address$2 pointer) near3 memory	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L20	90	output near2 queue near5 (address$2 pointer) near2 memory	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L21	21	output near2 queue near5 (address$2 pointer) near2 memory and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38

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L22	38	output near2 queue with (address$2 pointer) near3 memory and g06f$. ipc. not L21	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L23	551	address near2 queue with (address$2 pointer) near3 memory and g06f$.ipc. not L21	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L24	2	opcode near3 coprocessor with (send$3 transfer$4 transmit$4) with instruction	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L25	1791	receiv$3 near3 data same tempora$4 near3 stor$3 same process$3 near3 data same (transmi$5 send$3 pass$3) near4 data	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L26	22	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process$3 near3 data) same ((transmi$5 send$3 pass$3) near3 data with process$3) same (pipeline accelerat$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L27	1	((data near3 tempora$4 near3 stor$3) with (prior before) near3 process$3) same ((transmi$5 send$3 pass$3) same (pipeline accelerat$3))	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L28	658	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process$3 near3 data) same ((transmi$5 send$3 pass$3) near3 data with process$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L29	100	("register file") with ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L30	98	((processor pipeline) with memory with integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L31	108	((processor pipeline) with first near3 integrated adj circuit) and (memory DRAM) with (separate second) near3 integrated adj circuit	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L32	27	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) with (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L33	0	((processor pipeline) with memory with separate near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38
L34	48	("register file") near3 ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:38

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L35	59	(memory DRAM RAM) with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L36	49	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L37	3	((processor pipeline) with memory with separate near3 integrated adj circuit) same (faster speed failure)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L38	44	((processor pipeline) with memory with separate near3 integrated adj circuit) same advantag$4	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L39	219	((processor pipeline) with memory with separate near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L40	0	((processor pipeline) with memory with distinct near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L41	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (RAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L42	3	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L43	522	((processor pipeline) with memory with integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L44	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (DRAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L45	298	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L46	163	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L47	93	((processor pipeline) with memory with single near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

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L48	20	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (memory near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L49	1	((processor pipeline) with memory with (two multiple plurality) near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L50	24	((processor pipeline) with (DRAM RAM memory) with separate near2 chip) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L51	98	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L52	0	("register file") with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L53	71	L51 not L32	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L54	37	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L55	251	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L56	32010	buffer with ("integrated circuit" chip)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L57	30	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L58	48	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline CPU)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L59	6	buffer near3 separate near3 ("integrated circuit" chip) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L60	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

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L61	7	("2" two) near2 stage near3 (multiplier multiply multiplication) with latch	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L62	54	coprocessor with multipl$7 adj accumulat$3	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L63	42	multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L64	0	coprocessor same multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L65	26	pointer with "input buffer" and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L66	32	pointer with buffer with operand with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L67	313	pointer with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L68	8	pointer with buffer with input with (execution functional) near2 unit and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L69	44	pointer with next with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L70	54	pointer with buffer with input with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L71	196	pointer with buffer with (operand data) with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L72	10	read adj pointer with "input buffer" and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L73	142	read near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L74	155	read near3 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L75	31	(queue fifo) near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L76	18	queue near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L77	7	stor$3 near5 buffer near2 pointer near5 queue and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L78	31	queue near3 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L79	17	processor with coprocessor with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L80	141	"front end" with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

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L81	4	"front end" with separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L82	0	"front end" near3 separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L83	78	"front end" near3 separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L84	4	coprocessor with execut$3 with (division divide) near3 (operation instruction) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L85	370	712/34.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L86	270	712/35.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L87	437	712/200.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L88	683	712/225.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L89	1	"6282627".pn.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L90	3	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/14 11:39
L91	71	pipeline near2 accelerat$3	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2007/12/14 11:39
L92	12	("4991133" | "5619497" | "5991299" | "6317837" | "6408001" | "6434620" | "6496704" | "6498793" | "6661794" | "6687757" | "6757725" | "6789147").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 11:39
L93	7	L92 and header same $2processor	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 11:39
L94	5	coprocessor with message with header	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L95	157	tag with destination with register with (result data)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L96	10	L92 and header	US-PGPUB; USPAT; USOCR	OR	ON	2007/12/14 11:39

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L97	24	coprocessor with (packet instruction) with header	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L98	0	tag with destination with register with (result data) with coprocessor	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L99	67	huisman.xa.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L100	22	nakajima.in. and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L101	9	nakagoshi.in. and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L102	0	coprocessor with header with register with destination	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L103	3	coprocessor with (message packet) with register with destination	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L104	0	(PE "processing element") with message with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L105	6480	first near2 (PE element processor) same (second next) near2 (PE element processor) same (message packet data) with (transfer$4 transmit$4 pass$3 send$3)	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L106	1544	first near2 PE ("processing element") with second near2 (PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L107	0	first near2 (PE "processing element") with second near2 (PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L108	1544	first near2 PE ("processing element") with second near2 (PE "processing element") same header same result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L109	0	first near2 PE with second near2 PE with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L110	28	(PE "processing element") with message with result and "712"/$. ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L111	0	(PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39

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L112	48	first near2 (PE element processor) same (second next) near2 (PE element processor) same (message packet data) with (transfer$4 transmit$4 pass$3 send$3) same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L113	10	(PE "processing element") with among with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L114	1	(US-4985832-$).did.	USPAT	OR	ON	2007/12/14 11:39
L115	1	L114 and memory with message	USPAT	OR	ON	2007/12/14 11:39
L116	0	(PE "processing element") with amongst with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/14 11:39
L117	706	latch near2 memory near2 address	USPAT	OR	ON	2007/12/14 11:39
L118	474	latch near2 memory near2 address and (advantage benefit)	USPAT	OR	ON	2007/12/14 11:39
L119	1	latch near2 memory near2 address with (advantage benefit)	USPAT	OR	ON	2007/12/14 11:39
L120	49	latch with (provid$3 allow$3) with (synchronous synchronized) and g06f$.ipc.	USPAT	OR	ON	2007/12/14 11:39
L121	1	latch with (provid$3 allow$3) with (synchronous synchronized) same (advantage benefit)	USPAT	OR	ON	2007/12/14 11:39
L122	405	latch near2 (memory adj address)	USPAT	OR	ON	2007/12/14 11:39
L123	262	latch with (provid$3 allow$3) with (synchronous synchronized)	USPAT	OR	ON	2007/12/14 11:39
S1	86	pipeline near2 accelerator	US-PGPUB; USPAT	OR	ON	2006/06/19 11:11
S2	884	pipeline with accelerat$3	US-PGPUB; USPAT	OR	ON	2006/06/19 11:11
S3	220	pipeline near2 accelerat$3	US-PGPUB; USPAT	OR	ON	2006/10/03 13:45
S4	26	pipeline near2 accelerat$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/19 11:17
S5	0	accelerat$3 with load$3 with process$3 with external and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/19 11:17
S6	44	accelerat$3 with load$3 with process$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/20 08:19
S7	3	("5583964" "4956771" "5892962").pn.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:21
S8	10	mccarthy-paul.in.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:52

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S9	1	"5619430".pn.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:53
S10	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2006/06/20 10:54
S11	8	"raw data" with (coprocessor co-processor) same (buffer queue FIFO)	US-PGPUB; USPAT	OR	ON	2006/06/20 10:56
S12	31	"raw data" with (coprocessor co-processor)	US-PGPUB; USPAT	OR	ON	2006/06/20 14:51
S13	171	"raw data" with (slave PE DSP)	US-PGPUB; USPAT	OR	ON	2006/06/20 14:51
S14	9	"raw data" with (slave PE DSP) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/20 14:54
S15	12	"processed data" with (coprocessor co-processor) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/06/20 14:54
S16	1	(US-6624819-$).did.	USPAT	OR	ON	2006/06/21 08:41
S17	1	S16 and "160" with ("204" "206")	US-PGPUB; USPAT	OR	ON	2006/06/21 10:16
S18	165	output near2 queue with (address$2 pointer) near3 memory	US-PGPUB; USPAT	OR	ON	2006/06/21 10:22
S19	77	output near2 queue near5 (address$2 pointer) near2 memory	US-PGPUB; USPAT	OR	ON	2006/06/21 10:17
S20	19	output near2 queue near5 (address$2 pointer) near2 memory and g06f$.ipc.	US-PGPUB; USPAT	OR	ON	2006/06/21 10:17
S21	34	output near2 queue with (address$2 pointer) near3 memory and g06f$. ipc. not S20	US-PGPUB; USPAT	OR	ON	2006/06/21 11:06
S22	482	address near2 queue with (address$2 pointer) near3 memory and g06f$.ipc. not S20	US-PGPUB; USPAT	OR	ON	2006/06/21 10:22
S23	2	opcode near3 coprocessor with (send$3 transfer$4 transmit$4) with instruction	US-PGPUB; USPAT	OR	ON	2006/06/22 08:39
S30	1480	receiv$3 near3 data same tempora$4 near3 stor$3 same process$3 near3 data same (transmi$5 send$3 pass$3) near4 data	US-PGPUB; USPAT	OR	ON	2006/09/27 14:42
S31	538	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process$3 near3 data) same ((transmi$5 send$3 pass$3) near3 data with process$3)	US-PGPUB; USPAT	OR	ON	2006/09/27 14:43

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S32	5	(receiv$3 near3 data with tempora$4 near3 stor$3) same (process$3 near3 data) same ((transmi$5 send$3 pass$3) near3 data with process$3) same (pipeline accelerat$3)	US-PGPUB; USPAT	OR	ON	2006/09/27 14:45
S33	1	((data near3 tempora$4 near3 stor$3) with (prior before) near3 process$3) same ((transmi$5 send$3 pass$3) same (pipeline accelerat$3))	US-PGPUB; USPAT	OR	ON	2006/09/28 08:37
S34	84	((processor pipeline) with first near3 integrated adj circuit) and (memory DRAM) with (separate second) near3 integrated adj circuit	US-PGPUB; USPAT	OR	ON	2006/09/28 08:41
S35	177	((processor pipeline) with memory with separate near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:42
S36	38	((processor pipeline) with memory with separate near3 integrated adj circuit) same advantag$4	US-PGPUB; USPAT	OR	ON	2006/09/28 08:46
S37	3	((processor pipeline) with memory with separate near3 integrated adj circuit) same (faster speed failure)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:47
S38	0	((processor pipeline) with memory with separate near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:47
S39	0	((processor pipeline) with memory with distinct near3 integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:47
S40	73	((processor pipeline) with memory with integrated adj circuit) same (fail$3)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:51
S41	237	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/10/03 13:48
S42	41	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:54
S43	417	((processor pipeline) with memory with integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:54
S44	73	((processor pipeline) with memory with single near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2006/09/28 08:56

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S45	1	((processor pipeline) with memory with (two multiple plurality) near3 integrated adj circuit) same (benefi$5 advantag$6)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:25
S46	18	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (memory near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:27
S47	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (DRAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:27
S48	0	((processor pipeline) near5 (first second) near2 integrated adj circuit) same (RAM near5 (first second) near2 integrated adj circuit)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:27
S49	130	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:28
S50	3	((processor pipeline) near5 (first second) near2 chip) same ((RAM memory DRAM) near5 (first second) near2 chip) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:29
S51	15	((processor pipeline) with (DRAM RAM memory) with separate near2 chip) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:39
S52	85	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) same (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:43
S53	21	((processor pipeline) with (DRAM RAM memory) with (off-chip "off chip")) with (benefi$5 advantag$4)	US-PGPUB; USPAT	OR	ON	2006/09/28 09:41
S54	64	S52 not S53	US-PGPUB; USPAT	OR	ON	2006/09/28 10:12
S55	49	(memory DRAM RAM) with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2006/09/28 10:41
S56	0	("register file") with ("off chip" off-chip) with (cheap$2 expensive)	US-PGPUB; USPAT	OR	ON	2006/09/28 10:42
S57	86	("register file") with ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 10:43
S58	48	("register file") near3 ("off chip" off-chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 11:04

EAST Search History

S59	199	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory)	US-PGPUB; USPAT	OR	ON	2006/09/28 11:07
S60	22	((coprocessor accelerator DSP PE assist) with (read$3 receiv$3) with data with (buffer memory) with processor) same (process$3 near3 data) same (writ$3 send$3 transmit$4) with data with (buffer memory) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/28 11:59
S61	27742	buffer with ("integrated circuit" chip)	US-PGPUB; USPAT	OR	ON	2006/09/28 11:59
S62	6	buffer near3 separate near3 ("integrated circuit" chip) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2006/09/29 11:20
S63	34	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline)	US-PGPUB; USPAT	OR	ON	2006/09/28 12:01
S64	44	buffer near3 ((separate near3 ("integrated circuit" chip)) (off-chip "off chip")) with (processor pipeline CPU)	US-PGPUB; USPAT	OR	ON	2006/09/29 08:11
S65	1	"6205400".pn.	US-PGPUB; USPAT	OR	ON	2006/09/29 08:11
S66	7	("2" two) near2 stage near3 (multiplier multiply multiplication) with latch	US-PGPUB; USPAT	OR	ON	2006/09/29 11:23
S67	38	multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2006/09/29 11:28
S68	0	coprocessor same multiply adj accumulate with latch	US-PGPUB; USPAT	OR	ON	2006/09/29 11:28
S69	47	coprocessor with multipl$7 adj accumulat$3	US-PGPUB; USPAT	OR	ON	2006/09/29 13:10
S70	276	pointer with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2006/09/29 13:10
S71	38	pointer with next with data with "input buffer"	US-PGPUB; USPAT	OR	ON	2006/09/29 13:12
S72	7	read adj pointer with "input buffer" and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:14
S73	20	pointer with "input buffer" and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:16

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S74	3	pointer with buffer with input with (execution functional) near2 unit and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:18
S75	43	pointer with buffer with input with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:19
S76	151	pointer with buffer with (operand data) with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:19
S77	29	pointer with buffer with operand with read$3 and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:22
S78	125	read near3 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:23
S79	112	read near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:24
S80	24	queue near3 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:34
S81	13	queue near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:35
S82	25	(queue fifo) near2 pointer near3 buffer and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 13:38
S83	5	stor$3 near5 buffer near2 pointer near5 queue and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 15:43
S84	14	processor with coprocessor with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2006/09/29 16:26
S85	109	"front end" with separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2006/09/29 16:27
S86	61	"front end" near3 separate near3 (chip "integrated circuit")	US-PGPUB; USPAT	OR	ON	2006/09/29 16:27
S87	0	"front end" near3 separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/09/29 16:27
S88	4	"front end" with separate near3 (chip "integrated circuit") and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 09:34
S89	3	coprocessor with execut$3 with (division divide) near3 (operation instruction) and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 12:36
S90	319	712/34.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:02
S91	250	712/35.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:03
S92	405	712/200.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:04
S93	595	712/225.ccls.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:08

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S94	1	"6282627".pn.	US-PGPUB; USPAT	OR	ON	2006/10/02 15:08
S95	67	pipeline near2 accelerat$3	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/03 13:48
S96	3	((processor pipeline) with memory with (unique separate different) near3 integrated adj circuit)	USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/03 13:49
S97	4	coprocessor with message with header	US-PGPUB; USPAT	OR	ON	2007/05/04 10:46
S98	22	coprocessor with (packet instruction) with header	US-PGPUB; USPAT	OR	ON	2007/05/04 10:47
S99	12	("4991133" | "5619497" | "5991299" | "6317837" | "6408001" | "6434620" | "6496704" | "6498793" | "6661794" | "6687757" | "6757725" | "6789147").PN.	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/04 11:13
S100	10	S99 and header	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/04 11:13
S101	7	S99 and header same $2processor	US-PGPUB; USPAT; USOCR	OR	ON	2007/05/04 11:13
S102	155	tag with destination with register with (result data)	US-PGPUB; USPAT	OR	ON	2007/05/04 14:18
S103	0	tag with destination with register with (result data) with coprocessor	US-PGPUB; USPAT	OR	ON	2007/05/04 14:18
S105	67	huisman.xa.	US-PGPUB; USPAT	OR	ON	2007/12/12 16:11
S106	22	nakajima.in. and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/12 18:00
S107	9	nakagoshi.in. and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 10:57
S108	0	coprocessor with header with register with destination	US-PGPUB; USPAT	OR	ON	2007/12/13 10:57
S109	3	coprocessor with (message packet) with register with destination	US-PGPUB; USPAT	OR	ON	2007/12/13 11:01
S110	6480	first near2 (PE element processor) same (second next) near2 (PE element processor) same (message packet data) with (transfer$4 transmit$4 pass$3 send$3)	US-PGPUB; USPAT	OR	ON	2007/12/13 11:02

EAST Search History

S11 1	48	first near2 (PE element processor) same (second next) near2 (PE element processor) same (message packet data) with (transfer$4 transmit$4 pass$3 send$3) same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:10
S11 2	0	first near2 PE with second near2 PE with message same array and "712"/$:ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:10
S11 3	1544	first near2 PE ("processing element") with second near2 (PE "processing element") same header same result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:26
S11 4	1544	first near2 PE ("processing element") with second near2 (PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:27
S11 5	0	first near2 (PE "processing element") with second near2 (PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:27
S11 7	0	(PE "processing element") with message with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:28
S11 8	0	(PE "processing element") with header with result and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 11:28
S11 9	28	(PE "processing element") with message with result and "712"/$. ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 13:17
S12 0	10	(PE "processing element") with among with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 13:18
S12 1	0	(PE "processing element") with amongst with message same array and "712"/$.ccls.	US-PGPUB; USPAT	OR	ON	2007/12/13 13:18
S12 2	1	(US-4985832-$).did.	USPAT	OR	ON	2007/12/13 13:48
S12 3	1	S122 and memory with message	USPAT	OR	ON	2007/12/13 18:16
S12 4	706	latch near2 memory near2 address	USPAT	OR	ON	2007/12/13 18:17
S12 5	474	latch near2 memory near2 address and (advantage benefit)	USPAT	OR	ON	2007/12/13 18:17
S12 6	1	latch near2 memory near2 address with (advantage benefit)	USPAT	OR	ON	2007/12/13 18:17
S12 7	405	latch near2 (memory adj address)	USPAT	OR	ON	2007/12/13 18:20

EAST Search History

S128	262	latch with (provid$3 allow$3) with (synchronous synchronized)	USPAT	OR	ON	2007/12/13 18:21
S129	1	latch with (provid$3 allow$3) with (synchronous synchronized) same (advantage benefit)	USPAT	OR	ON	2007/12/13 18:21
S130	49	latch with (provid$3 allow$3) with (synchronous synchronized) and g06f$.ipc.	USPAT	OR	ON	2007/12/13 18:22